

**AMENDMENTS TO THE CLAIMS**

Listing of the claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

1. (Canceled)

2. (Currently Amended) A semiconductor integrated circuit, comprising:

a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further pair of transistors including a third MOS transistor and a fourth MOS transistor, connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and

a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit and generating a differential amplification output signal,

wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal, and wherein the gate of each transistor has a gate length and a gate width, the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is about three times or less than the ratio between

the gate length and the gate width of the other one of the transistors in the pair of the series-connected MOS transistors such that fluctuation of a voltage level of the differential amplification output signal is suppressed and fluctuation of delay time of the differential amplification output signal is in a predetermined time period regardless of a change in voltage levels of the first and second input signals.

3. (Previously Presented) The semiconductor integrated circuit according to claim 2, wherein the gate of each transistor has a gate length and a gate width, and the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is substantially the same as the ratio between the gate length and the gate width of the other one of the transistors in the pair of the series-connected MOS transistors.

4. (Previously Presented) The semiconductor integrated circuit according to claim 2, wherein each transistor has a gain constant, and the gain constant of one of the transistors in each pair of the series-connected MOS transistors is substantially the same as the gain constant of the other one of the transistors in the pair of the series-connected MOS transistors.

5. (Previously Presented) The semiconductor integrated circuit according to claim 2, wherein each transistor has a channel length modulation constant, and the channel length modulation constant of one of the transistors in each pair of the series-connected MOS transistors is substantially the same as the channel length modulation

constant of the other one of the transistors in the pair of the series-connected MOS transistors.

6. (Previously Presented) The semiconductor integrated circuit according to claim 2, wherein the differential amplification circuit is connected between the first power supply and the second power supply.

7. (Currently Amended) ~~A semiconductor integrated circuit, comprising:  
a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further pair of transistors including a third MOS transistor and fourth MOS transistor, connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and~~

~~a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit,~~

~~wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal, and~~  
The semiconductor integrated circuit according to claim 2, wherein the first to fourth

MOS transistors each include a source and a back gate, which is connected to the source.

8. (Previously Presented) A semiconductor integrated circuit, comprising:
  - a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further pair of transistors including a third MOS transistor and a fourth MOS transistor connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and
  - a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit,
- wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal, and
- wherein the differential amplification circuit includes a plurality of MOS transistors, each having a gate provided with a predetermined gate voltage capacity, the semiconductor device further comprising:
  - a fifth MOS transistor connected between the differential amplification circuit and the node connecting the first and second MOS transistors; and

a sixth MOS transistor connected between the differential amplification circuit and the node connecting the third and fourth MOS transistors, the fifth and sixth MOS transistors each having a gate to which voltage less than the gate voltage capacity of each MOS transistor in the differential amplification circuit is applied.

9. (Previously Presented) A semiconductor integrated circuit, comprising:

a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further pair of transistors including a third MOS transistor and a fourth MOS transistor, connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and

a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit,

wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal, and wherein the level conversion circuit includes:

a fifth MOS transistor having a gate for receiving a current restriction signal, a source connected to one of the first and second power supplies, and a drain connected to the gates of the first and fourth MOS transistors;

a sixth MOS transistor having a gate for receiving the current restriction signal, a source connected to one of the first and second power supplies, and a drain connected to the gates of the second and third MOS transistors.

10. (Original) The semiconductor integrated circuit according to claim 9, wherein the level conversion circuit includes:

a seventh MOS transistor, connected to one of the first and second power supplies, for fixing voltage to a predetermined value at the node connecting the first MOS transistor and the second MOS transistor; and

an eighth MOS transistor, connected to one of the first and second power supplies, for fixing voltage to a predetermined value at the node connecting the third MOS transistor and the fourth MOS transistor.

11. (Previously Presented) A semiconductor integrated circuit, comprising:

a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further pair of transistors including a third MOS transistor and a fourth MOS transistor, connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and

a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit,

wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal, and wherein the first to fourth MOS transistors are each N-type conduction transistors, and potential at one of the first and second power supplies is lower than potential at the other one of the first and second power supplies, the level conversion circuit including:

an N-type fifth MOS transistor having a gate for receiving a current restriction signal, a source connected to the one of the first and second power supplies at which the potential is lower, and a drain connected to the gates of the first and fourth MOS transistors; and

an N-type sixth MOS transistor having a gate for receiving the current restriction signal, a source connected to the one of the first and second power supplies at which the potential is lower, and a drain connected to the gates of the second and third MOS transistors.

12. (Previously Presented) A semiconductor integrated circuit, comprising:

a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further pair of transistors including a third MOS transistor and a fourth MOS transistor, connected in series between the first

power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and

a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit,

wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal, and wherein the first to fourth MOS transistors are each P-type conduction transistors, and potential at one of the first and second power supplies is greater than potential at the other one of the first and second power supplies, the level conversion circuit including:

a P-type fifth MOS transistor having a gate for receiving a current restriction signal, a source connected to the one of the first and second power supplies at which the potential is greater, and a drain connected to the gates of the first and fourth MOS transistors; and

a P-type sixth MOS transistor having a gate for receiving the current restriction signal, a source connected to the one of the first and second power supplies at which the potential is greater, and a drain connected to the gates of the second and third MOS transistors.



13. (Previously Presented) A semiconductor integrated circuit, comprising:

a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further pair of transistors including a third MOS transistor and a fourth MOS transistor, connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and

a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit,

wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal, and wherein the differential amplification circuit includes a plurality of MOS transistors, each provided with a predetermined gate voltage capacity, the first to fourth MOS transistors of the level conversion circuit each being provided with a gate voltage capacity that is greater than the gate voltage capacity of each MOS transistor in the differential amplification circuit.

14. (Previously Presented) A semiconductor integrated circuit, comprising:

a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power

supply and a second power supply, and a further pair of transistors including a third MOS transistor and a fourth MOS transistor, connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and

a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit,

wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal, and wherein potential at one of the first and second power supplies is greater than potential at the other one of the first and second power supplies, and the differential amplification circuit is connected to the one of the first and second power supplies at which the potential is greater;

wherein the differential amplification circuit includes a plurality of MOS transistors, each provided with a predetermined gate voltage capacity, the first to fourth MOS transistors of the level conversion circuit each being provided with a gate voltage capacity that is greater than the gate voltage capacity of each MOS transistor in the differential amplification circuit; and

wherein the level conversion circuit receives an input signal having voltage greater than the greater one of the potentials at the first and second power supplies.

15. (Currently Amended) A semiconductor integrated circuit comprising:

a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further pair of transistors including a third MOS transistor and a fourth MOS transistor, connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and

a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit and generating a differential amplification output signal,

wherein the gate of each transistor has a gate length and a gate width, the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is about three times or less than the ratio between the gate length and the gate width of the other one of the transistors in each pair of the series-connected MOS transistors such that fluctuation of a voltage level of the differential amplification output signal is suppressed and fluctuation of delay time of the differential amplification output signal is in a predetermined time period regardless of a change in voltage levels of the first and second input signals.

16. (Original) The semiconductor integrated circuit according to claim 15, wherein the first and fourth MOS transistors each receive a first input signal, and the

second and third MOS transistors each receive a second input signal having a phase inverted from the phase of the first input signal.

17-20. (Canceled).